Lab 8: Mod-13 Up/Down counter SV test bench

DUT and SV testbench is

<https://drive.google.com/drive/folders/1JlAUhaLeWjG3bMuQ1HYuZiS1WXBaiMaX?usp=drive_link>

Make changes to design.sv, testbench.sv, interface.sv,transaction.sv,driver.sv,monitor.sv,scoreboard.sv as per below instructions

Goal

* Update DUT to do both up/down counting Add additional input signal up\_dwn and modify DUT to up count if this input is 1, and down count if 0
* Modify interface.sv to add new port
* Modify testbench.sv to connect new port of DUT
* Modify transaction.sv to add new input port as random
* Modify transaction.sv function to print UP/DOWN counter mode
* Modify driver.sv to send new input to DUT
* Modify monitor.sv to reflect new input
* Scoreboard.sv: add scoreboard logic corresponding to DUT functionality. Currently it contains just a template / place holder
* Run simulation, review log and waveform, make sure up and down counting is working as expected

Submit RTL file, modified testbench, log and waveform